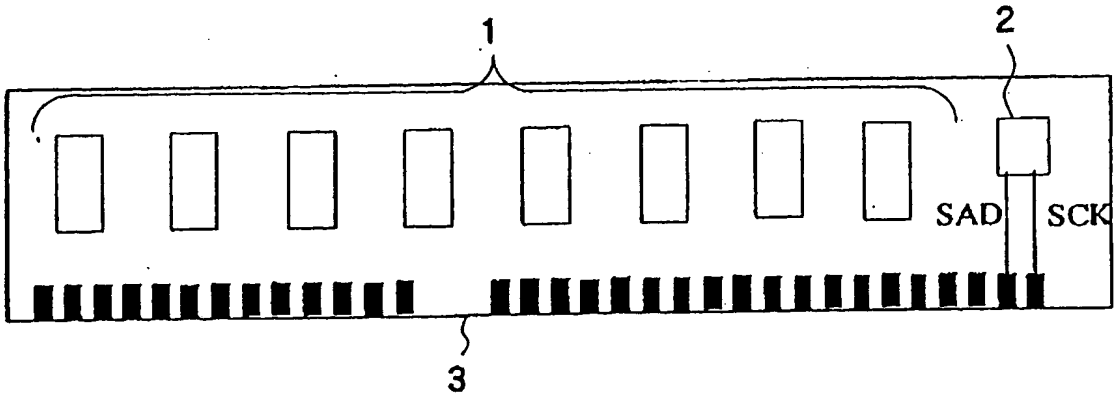

FIG. 1 (PRIOR ART)

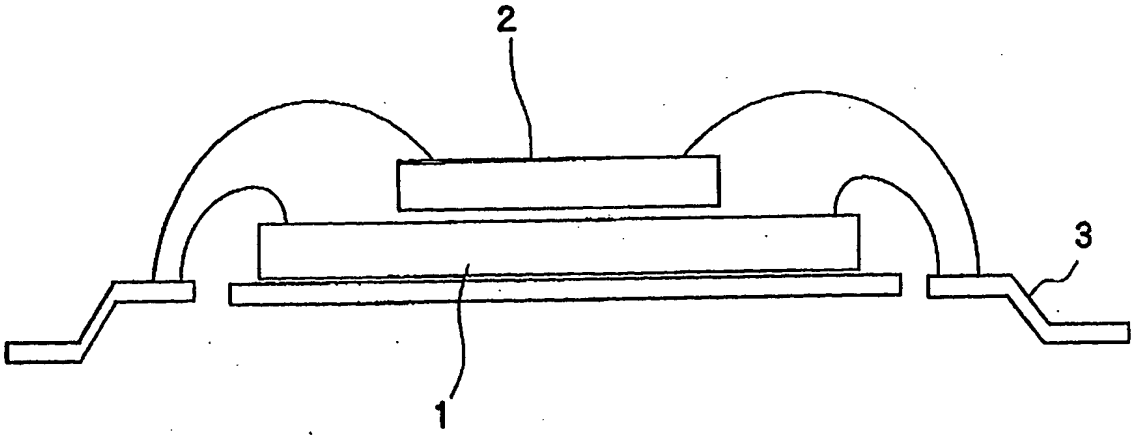

FIG. 2 (PRIOR ART)

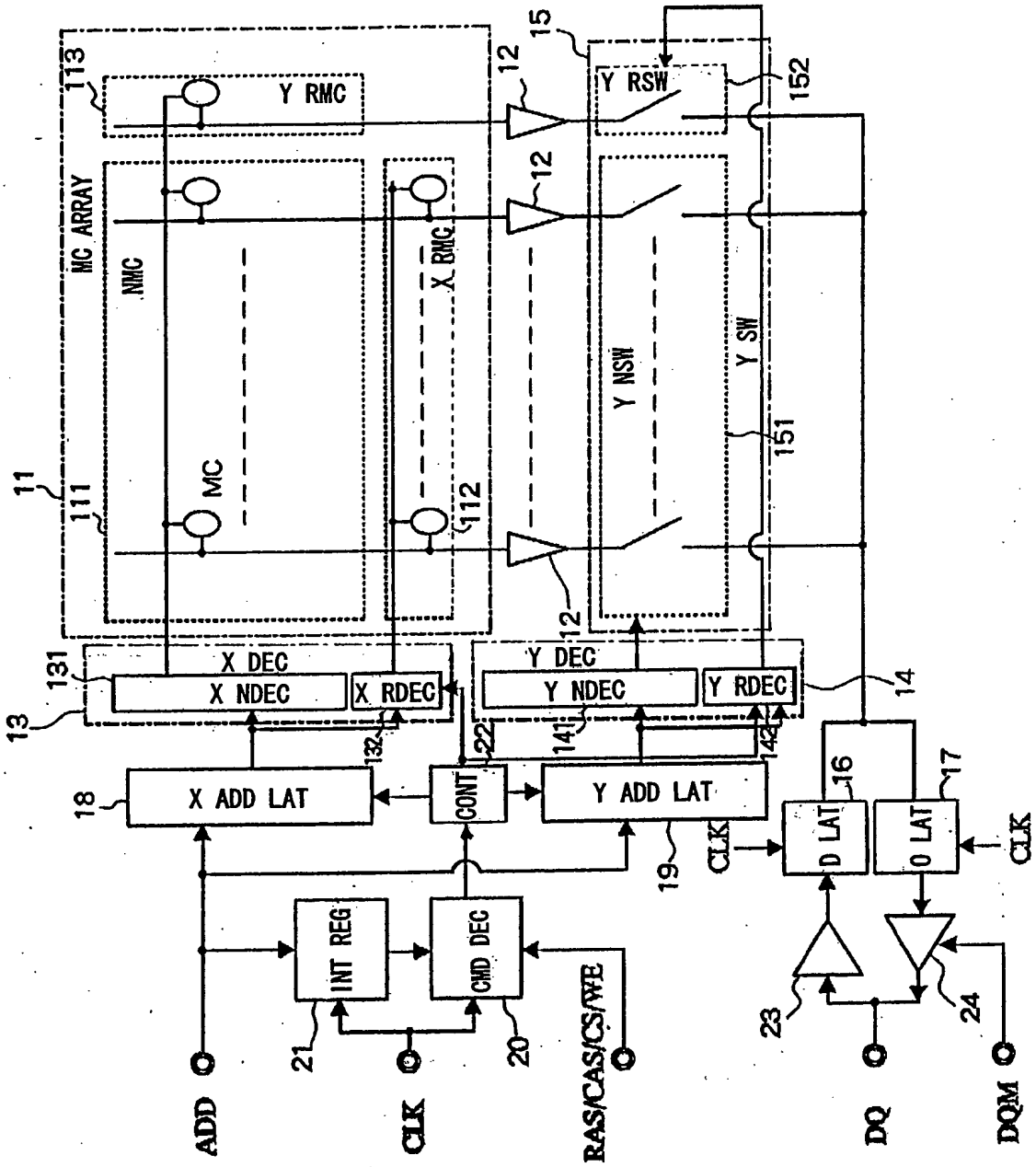

FIG. 3 (PRIOR ART)

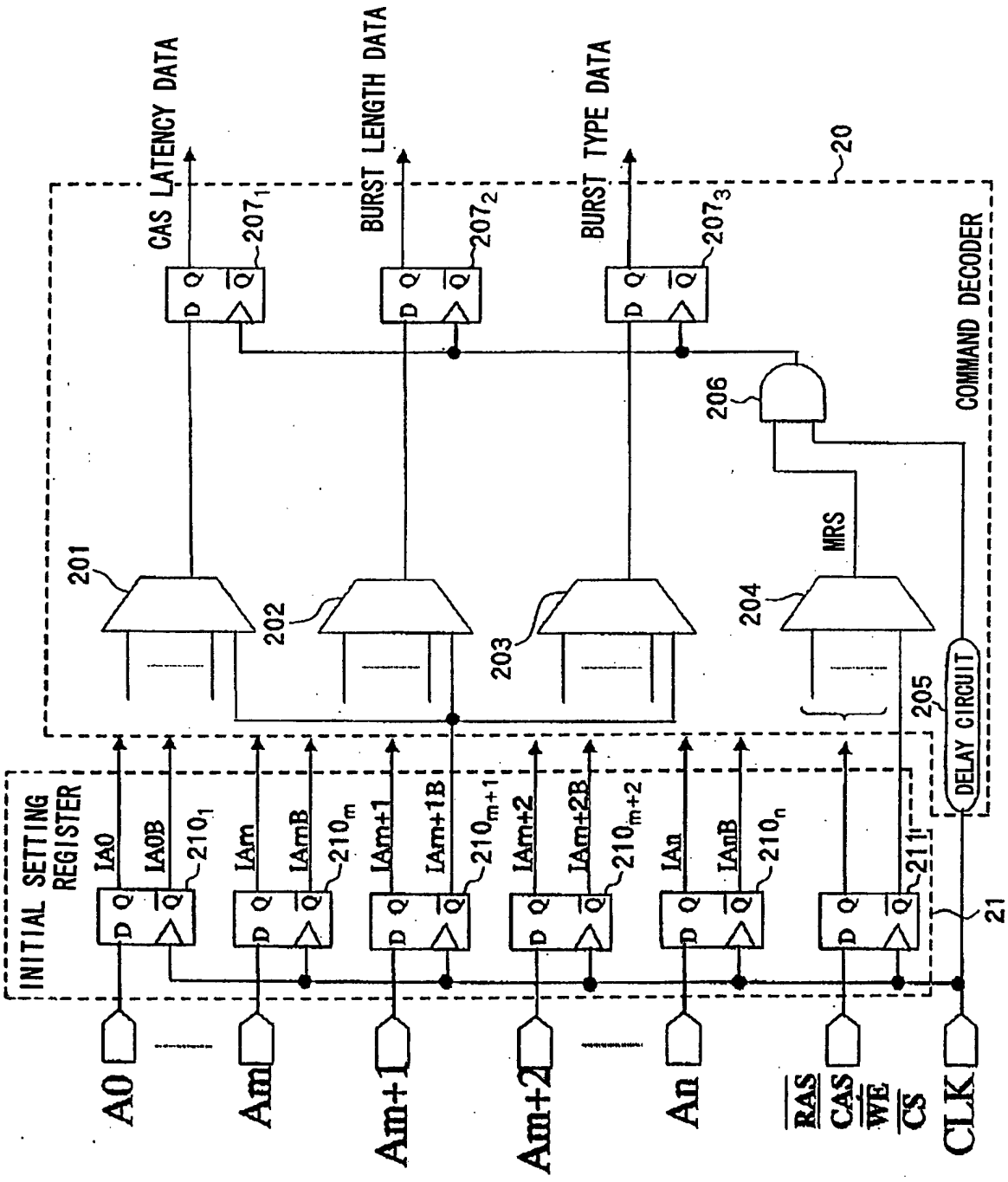

FIG. 4 (PRIOR ART)

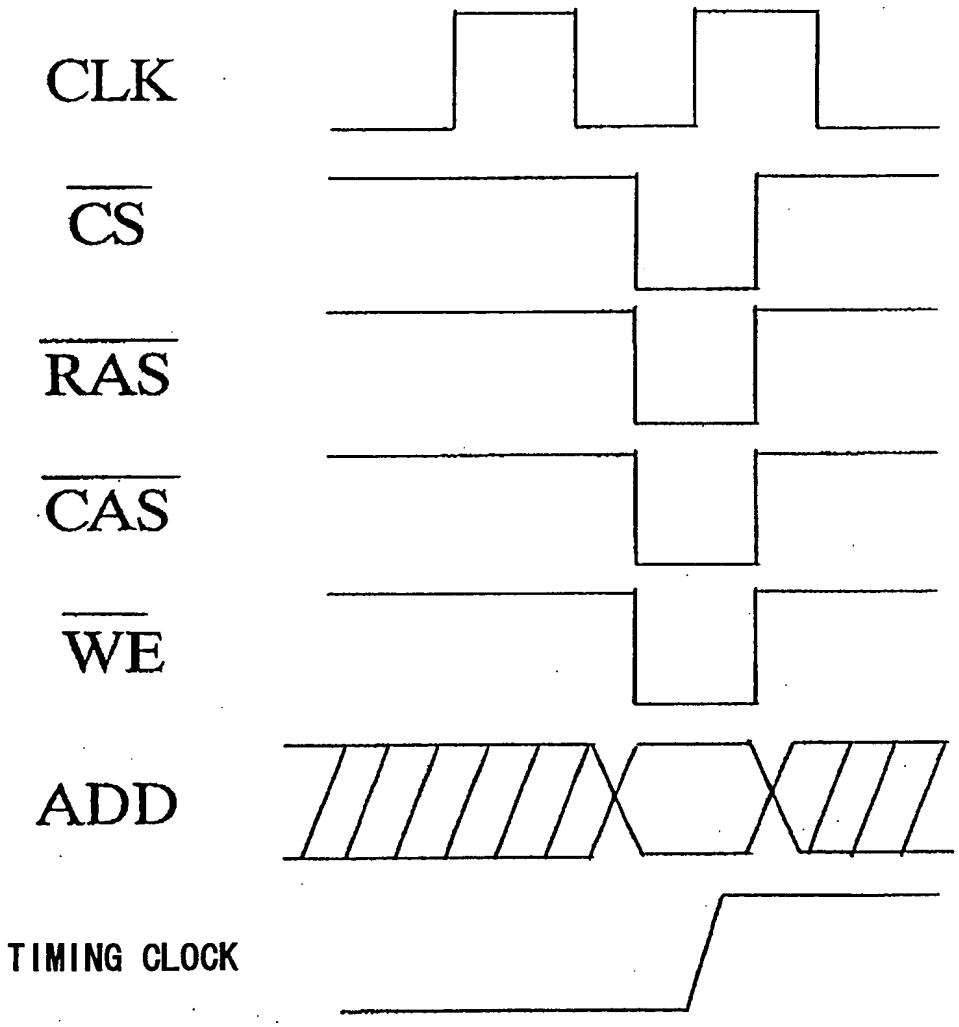

FIG. 5 (PRIOR ART)

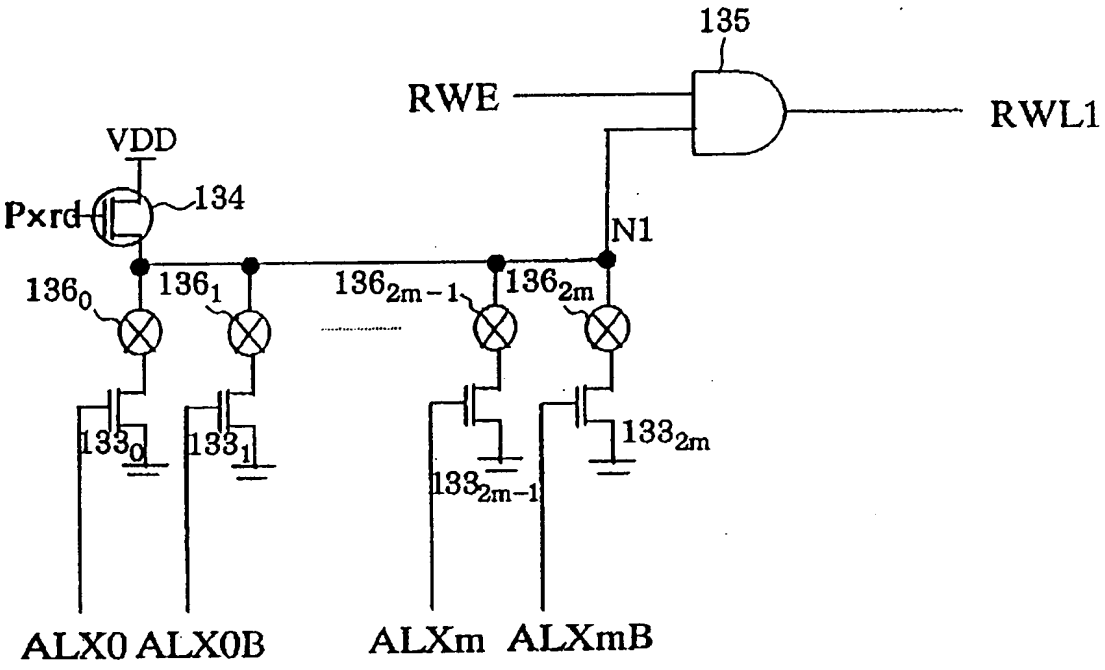

FIG. 6 (PRIOR ART)

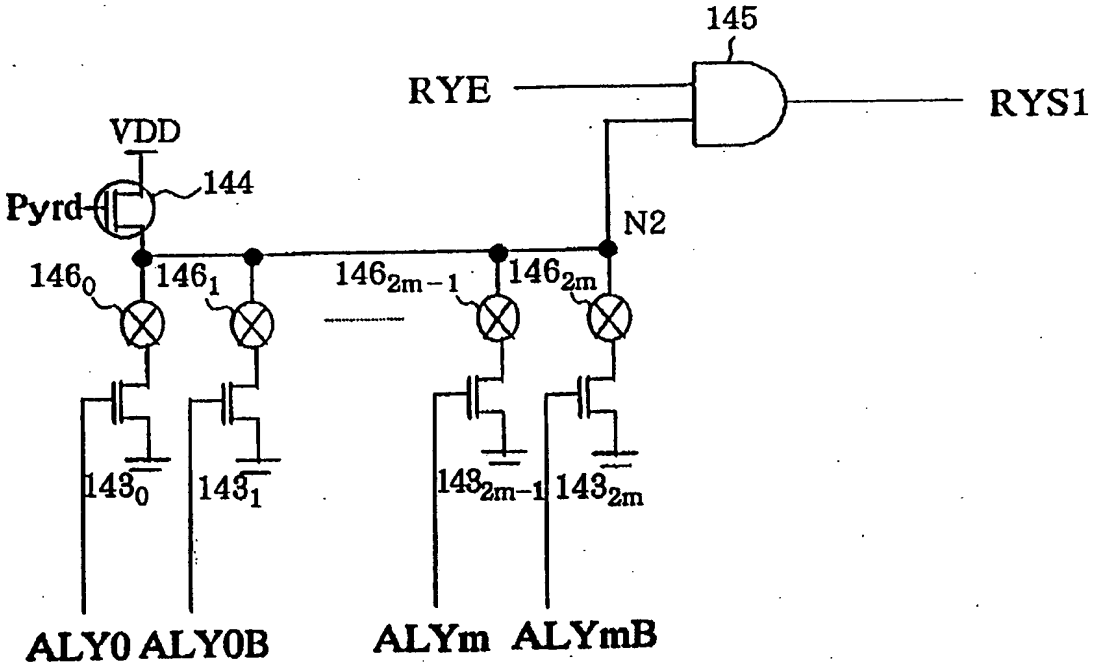

FIG. 7 (PRIOR ART)

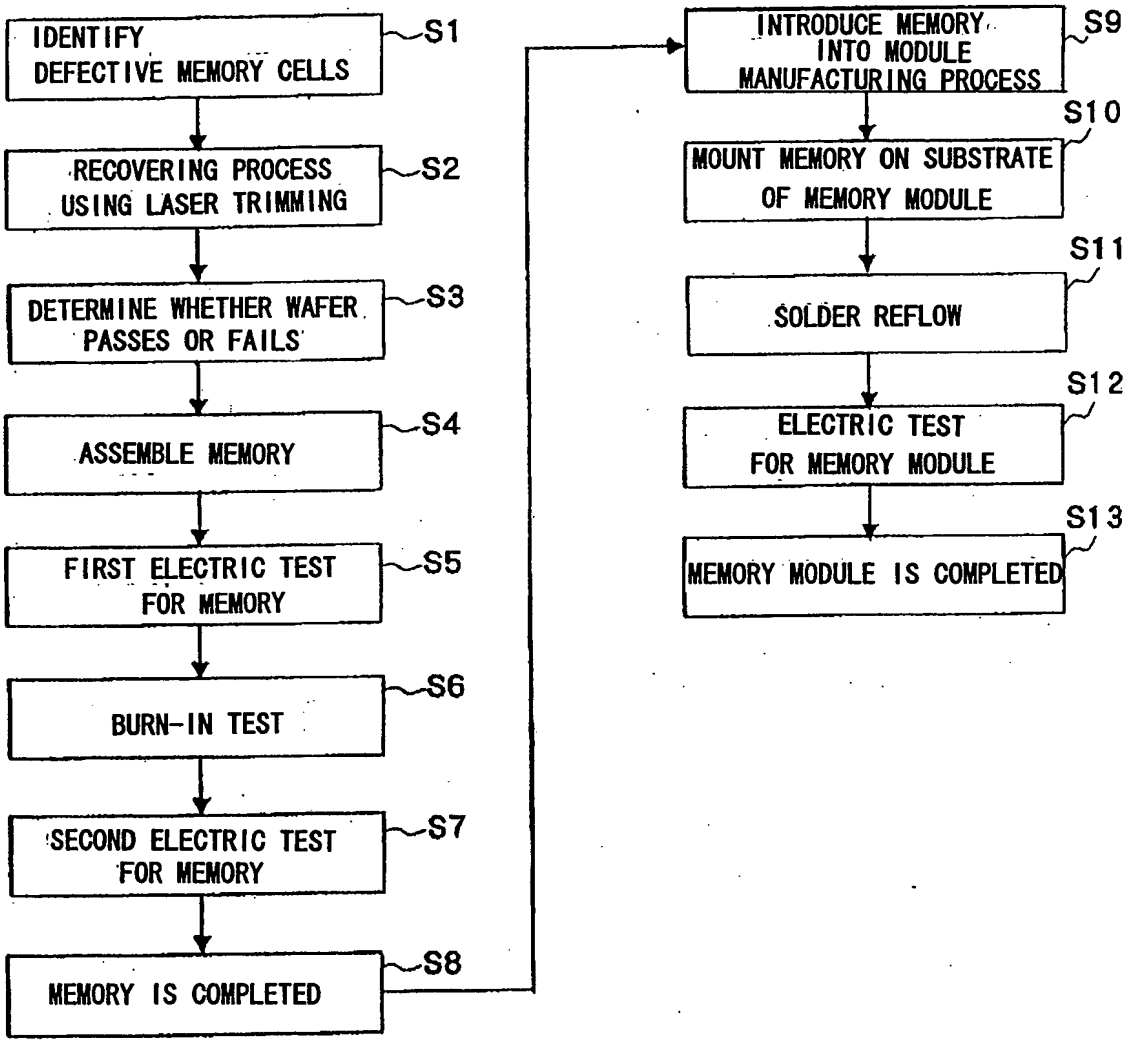

FIG. 8 (PRIOR ART)

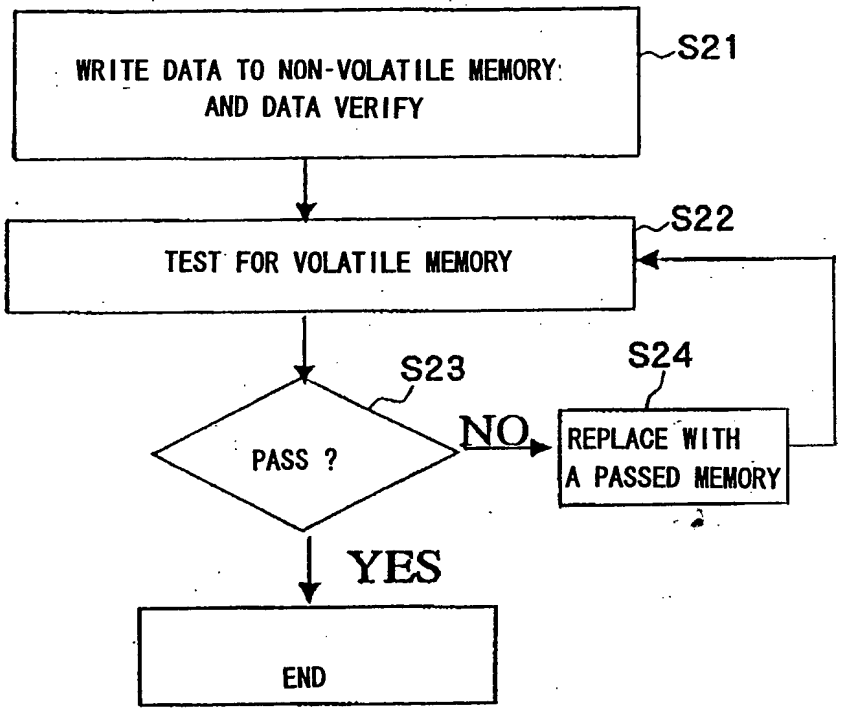

FIG. 9 (PRIOR ART)

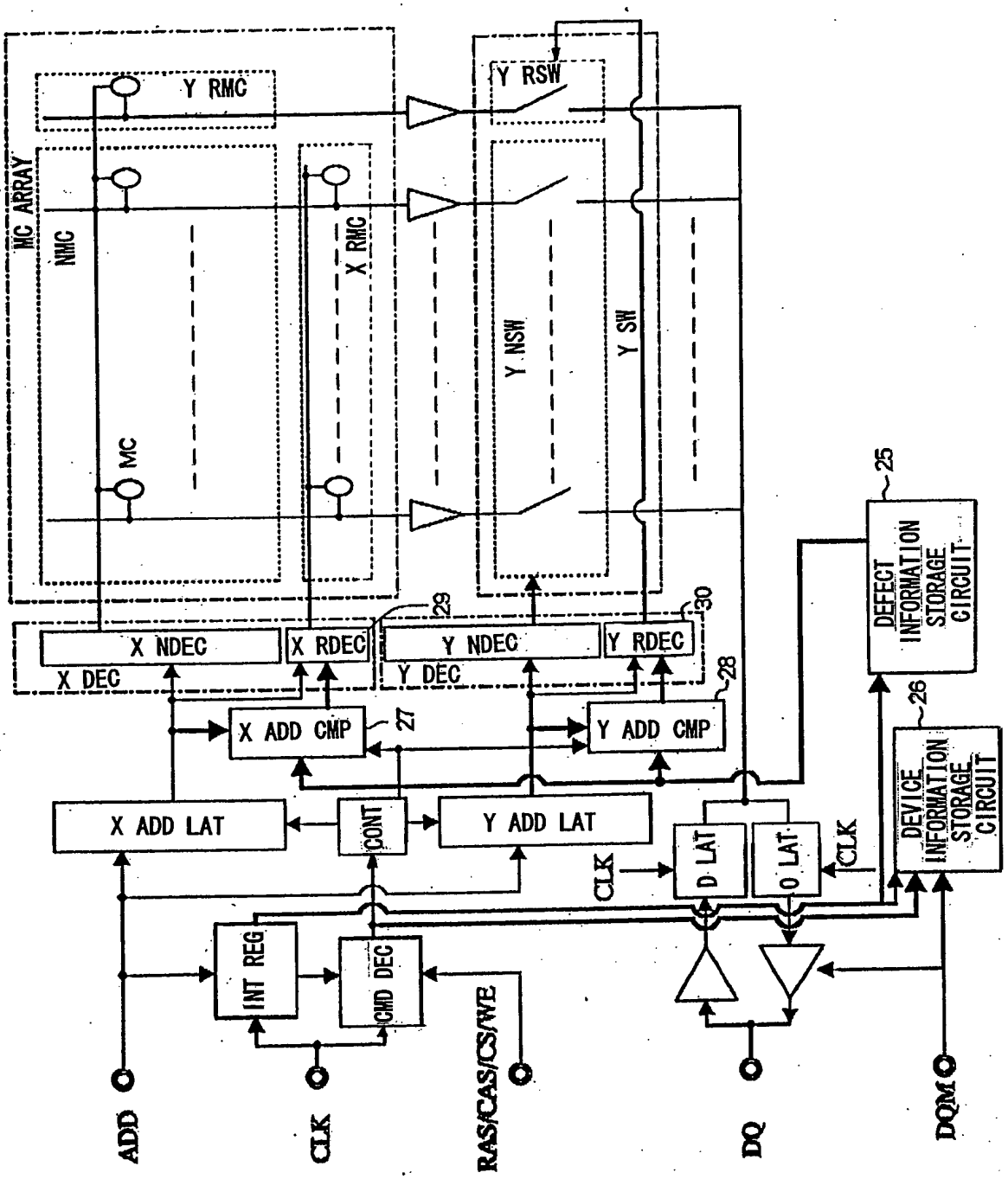
MC ARRAY
NMC
MC
Y RMC
X RMC
Y RSW
Y NSW
Y SW
X NDEC
X RDEC
X DEC
Y NDEC
Y RDEC
Y DEC
29
30
28
X ADD CMP
27
Y ADD CMP
X ADD LAT
CONT
Y ADD LAT
D LAT
Q LAT
CLK
CLK
INT REG
CMD DEC
25
DEFECT INFORMATION STORAGE CIRCUIT
26
DEVICE INFORMATION STORAGE CIRCUIT
ADD
CLK
RAS/CAS/CS/WE
DQ
DQM

FIG. 10

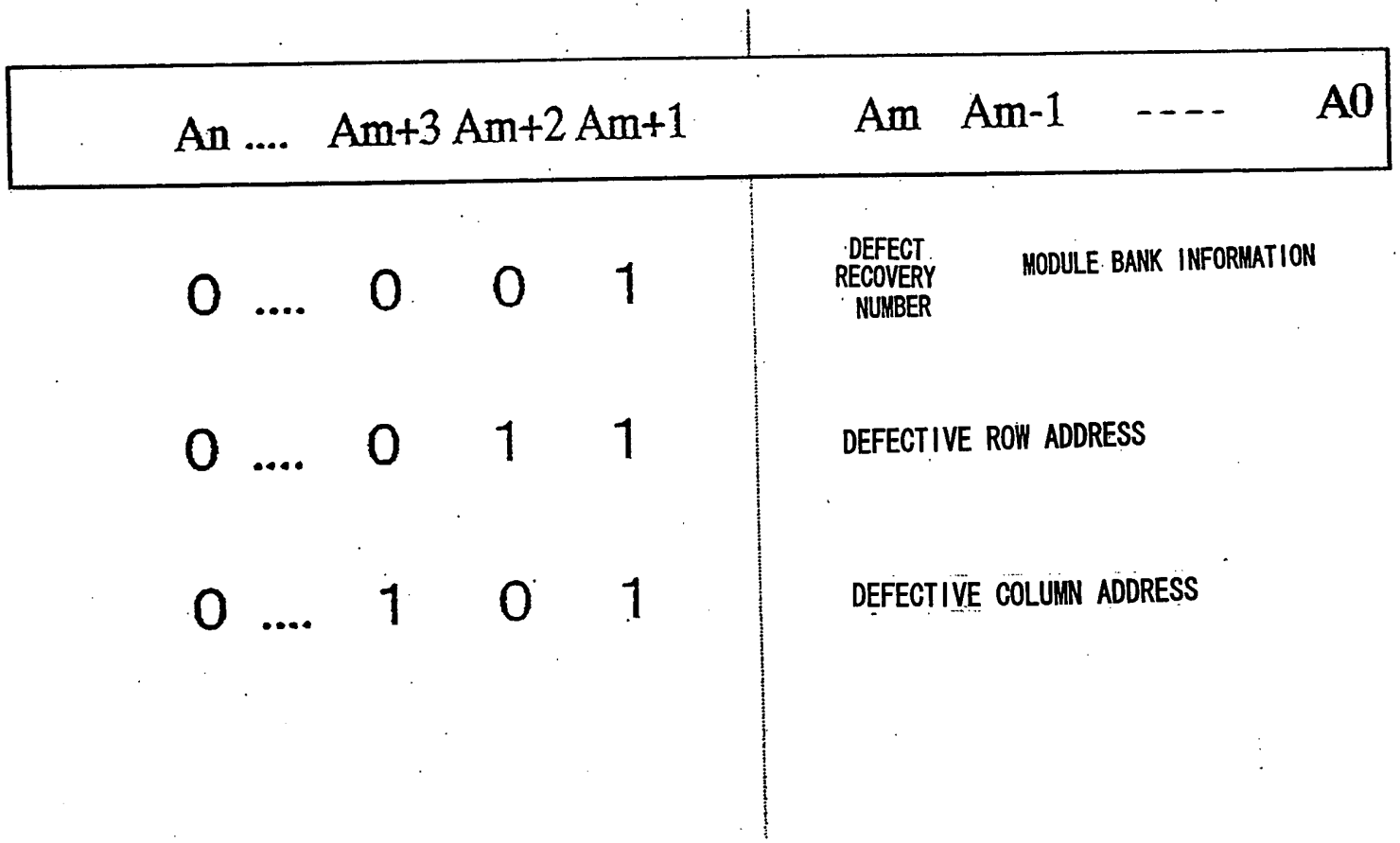
An .... Am+3 Am+2 Am+1
Am Am-1 ---- A0
0 .... 0 0 1
DEFECT RECOVERY NUMBER
MODULE BANK INFORMATION
0 .... 0 1 1
DEFECTIVE ROW ADDRESS
0 .... 1 0 1
DEFECTIVE COLUMN ADDRESS

FIG. 11

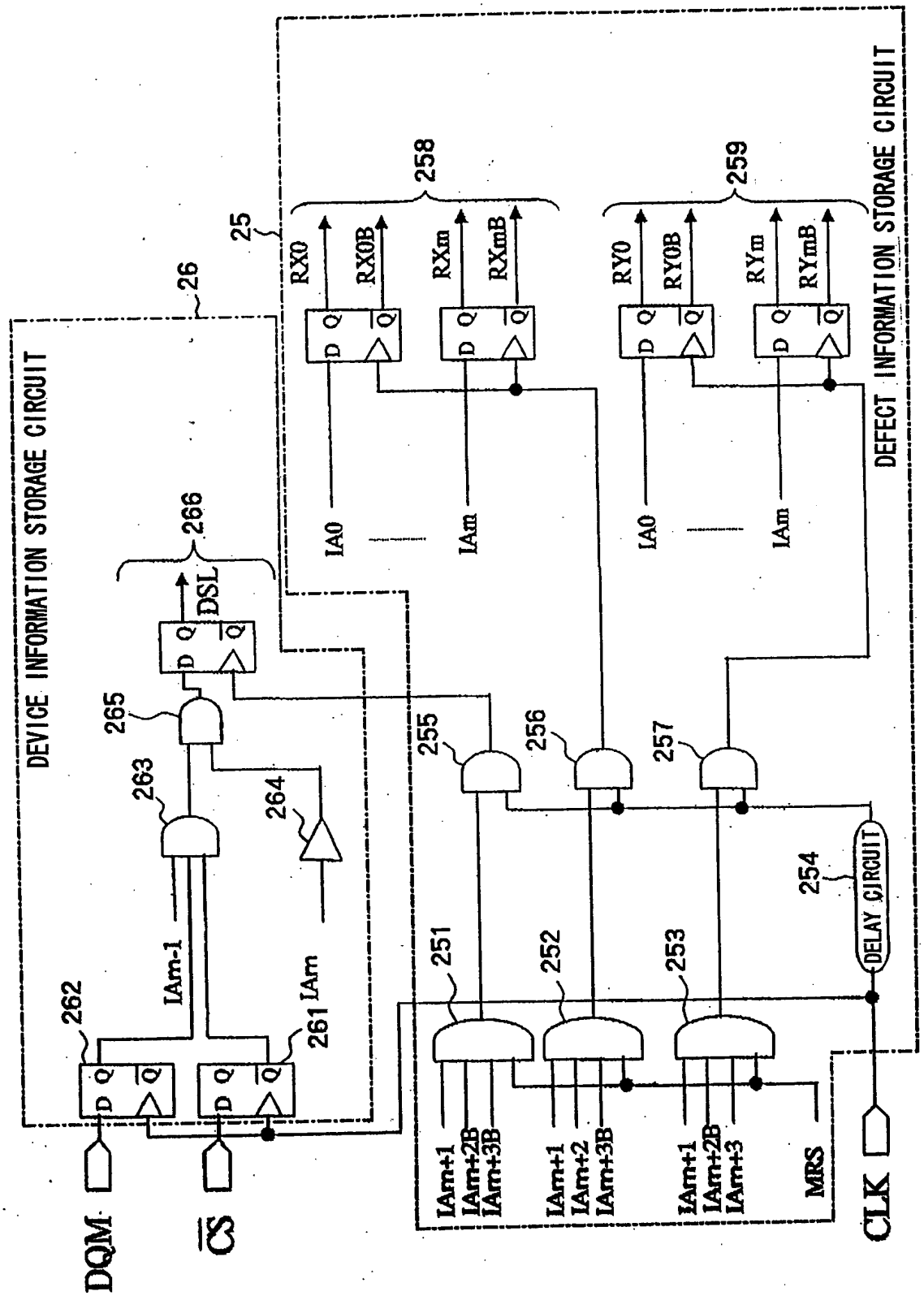
DEVICE INFORMATION STORAGE CIRCUIT
DEFECT INFORMATION STORAGE CIRCUIT
DELAY CIRCUIT
DQM
CS
CLK
MRS
DSL
RX0
RX0B
RXm
RXmB
RY0
RY0B
RYm
RYmB
IA0
IAm
IAm-1
IAm+1
IAm+2B
IAm+3B
IAm+2
IAm+3
25
26
251
252
253
254
255
256
257
258
259
261
262
263
264
265
266

FIG. 12

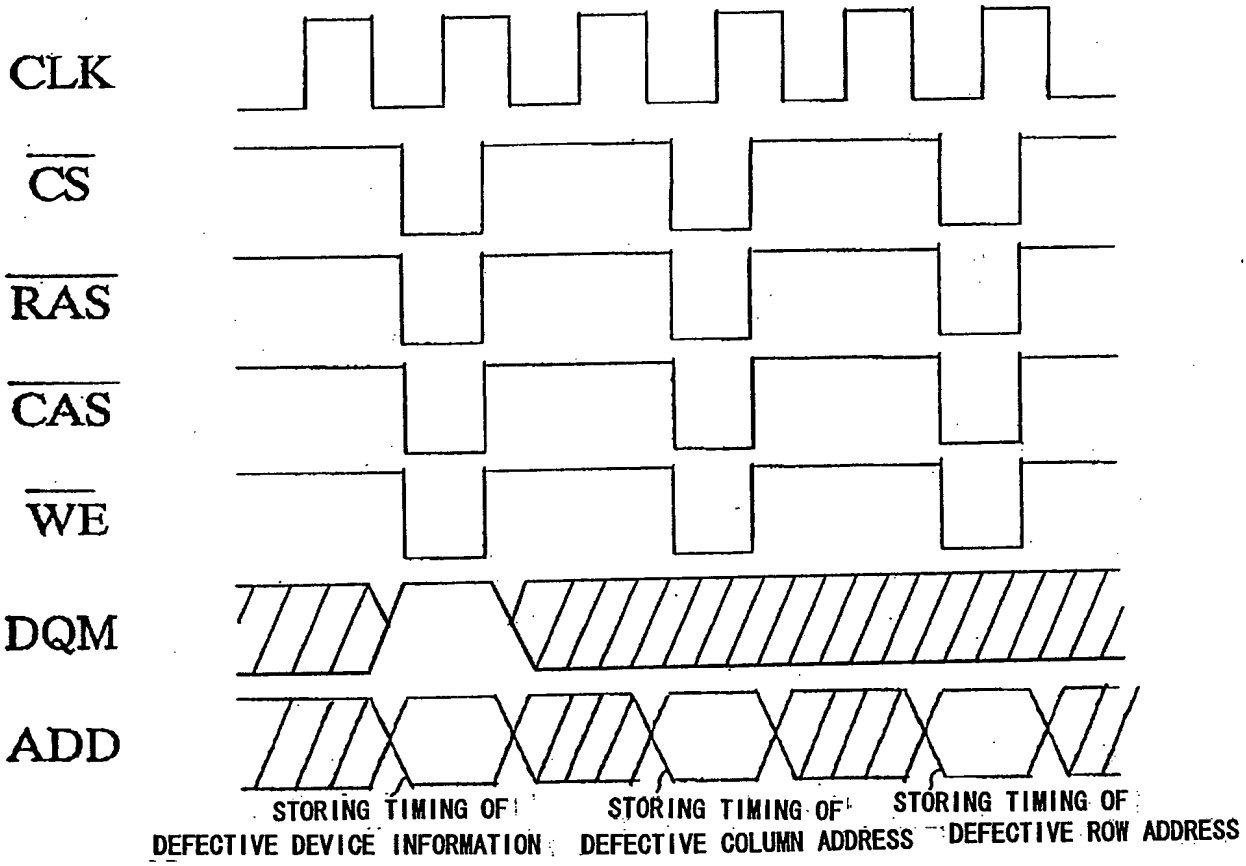
CLK
$\overline{CS}$
$\overline{RAS}$
$\overline{CAS}$
$\overline{WE}$
DQM
ADD
STORING TIMING OF DEFECTIVE DEVICE INFORMATION
STORING TIMING OF DEFECTIVE COLUMN ADDRESS
STORING TIMING OF DEFECTIVE ROW ADDRESS

FIG. 13

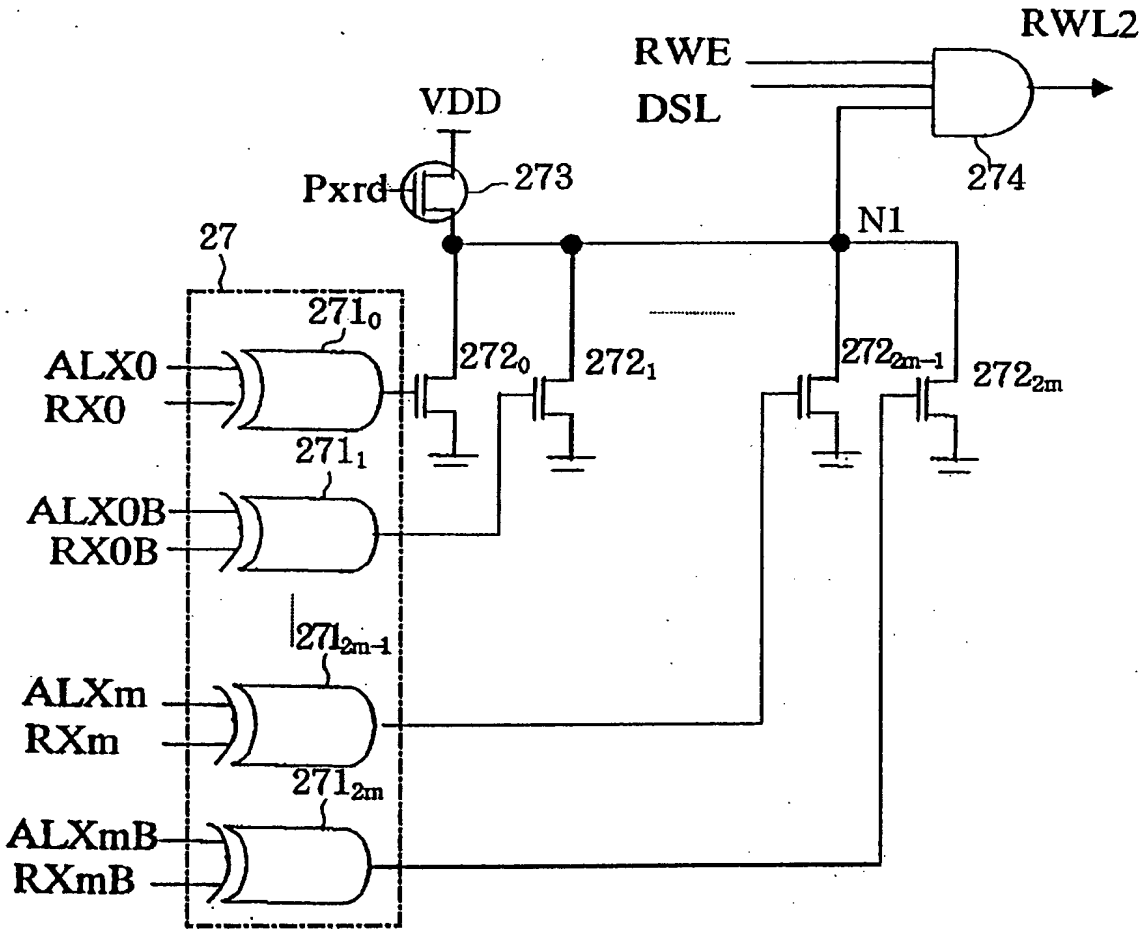
RWL2
RWE
DSL
VDD
Pxrd
273
274
N1
27
271_0
272_0
272_1
272_{2m-1}
272_{2m}
ALX0
RX0
271_1
ALX0B
RX0B
271_{2m-1}
ALXm
RXm
271_{2m}
ALXmB
RXmB

FIG. 14

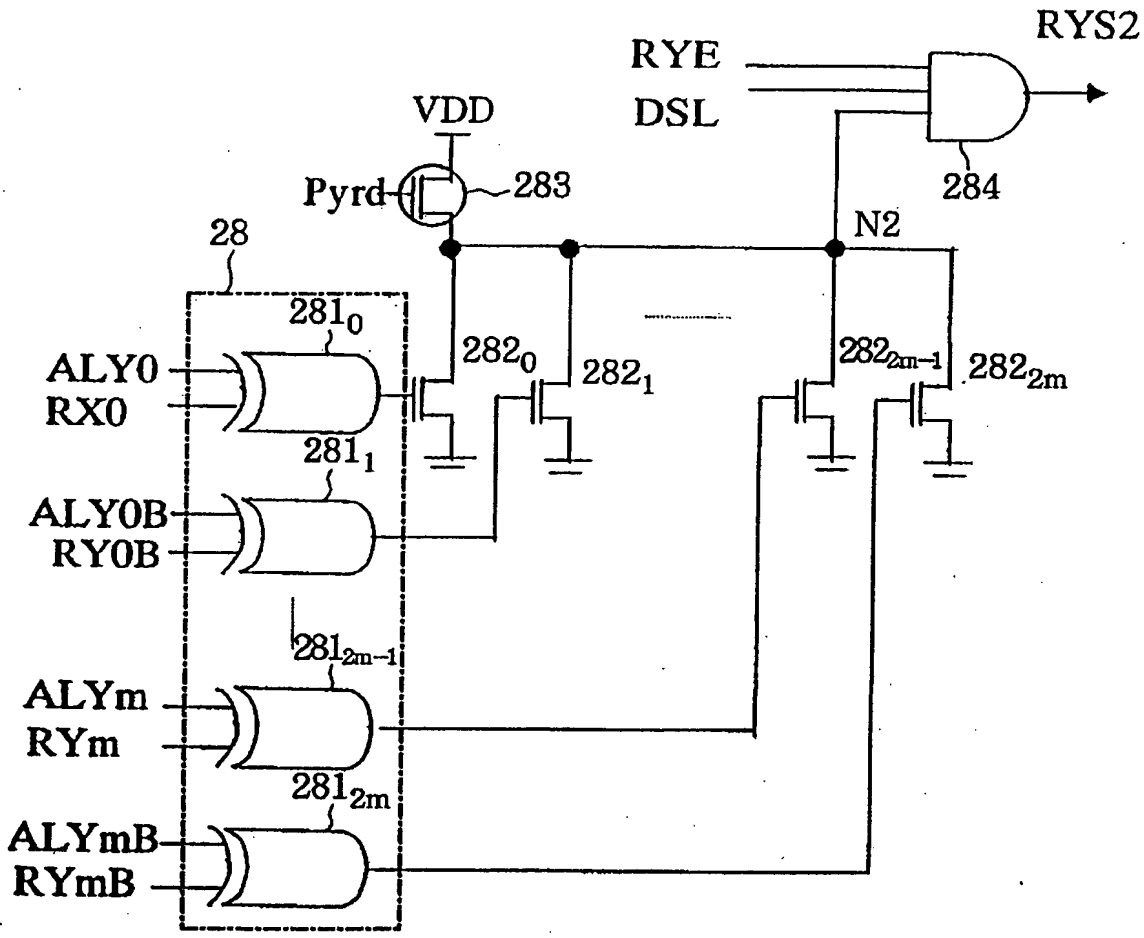
RYS2
RYE
DSL
VDD
Pyrd
283
284
N2
28
281_0
282_0
282_1
282_{2m-1}
282_{2m}
ALY0
RX0
281_1
ALY0B
RY0B
281_{2m-1}
ALYm
RYm
281_{2m}
ALYmB
RYmB

FIG. 15

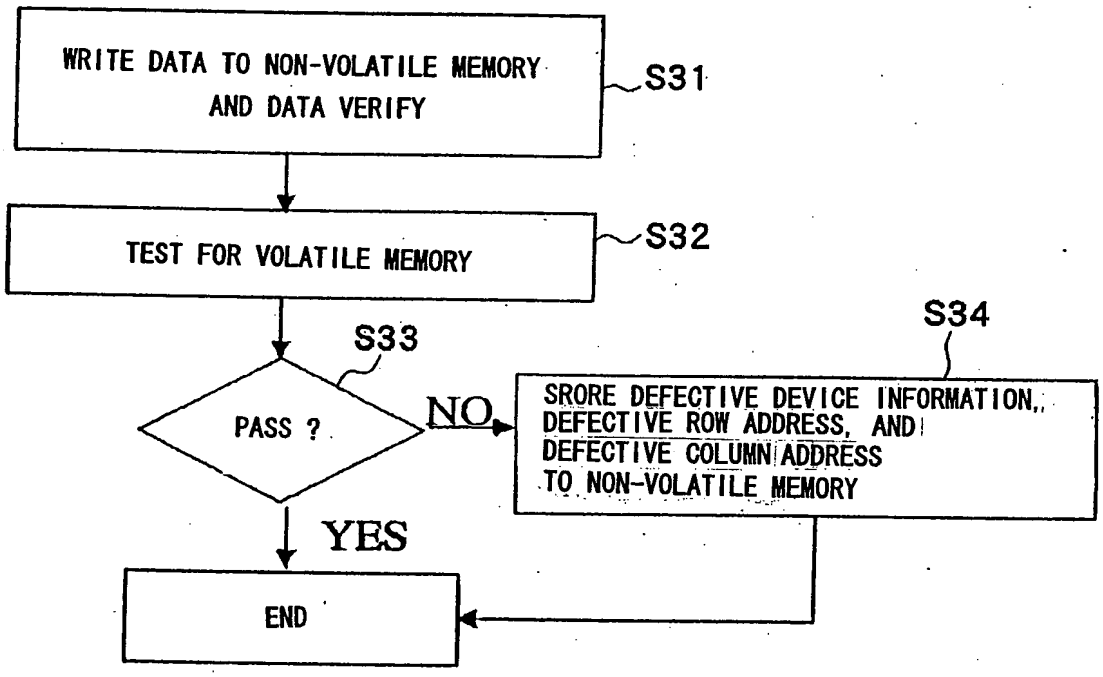
WRITE DATA TO NON-VOLATILE MEMORY AND DATA VERIFY
S31
TEST FOR VOLATILE MEMORY
S32
S33
PASS ?
NO
S34
SRORE DEFECTIVE DEVICE INFORMATION, DEFECTIVE ROW ADDRESS, AND DEFECTIVE COLUMN ADDRESS TO NON-VOLATILE MEMORY
YES
END

FIG. 16